Chapter 5. North American Cellular System Based on Time Division Multiple Access
Background and Goals

- AMPS can not support user transparency roaming
- Interim Standard 41 (IS 41) is to deliver AMPS services to roaming subscribers
- IS-54 was created after GSM, it support dual mode access capability (analog and digital transmission)
- IS-136 is a revised version of IS-54. We refer to the system as NA-TDMA
Architecture

- NA-TDMA is an extension of AMPS
- IS-136 systems are capable of operating with AMPS terminals, dual mode terminals, and all-digital terminals
- NA-TDMA specifies three types of external network:
  - Public systems: terminal as a cellular phone
  - Residential systems: terminal as a cordless phone
  - Private systems: terminal as a business phone
Figure 5.1 NA-TDMA architecture.
Architecture

• NA-TDMA defines a large number of ID codes including all of the AMPS codes:
  – 64-bit Encryption Key (A-Key)
  – 12-bit location area identifier (LOCAID): the system can divide its service area into clusters of cells referred to as location areas
  – The 12-bit digital verification code (DVCC) plays the same role in digital traffic channel as the SAT
Radio Transmission

- IS-136 specifies dual mode NA-TDMA/AMPS operation in the AMPS frequency bands.
- Each band of NA-TDMA specifies carriers spaced at 30 kHz. Each pair of NA-TDMA carriers corresponds to an AMPS channel.
- The access technology conforms to the hybrid FDMA/TDMA.
- Each frame contains six time slots and the frame duration is 40 ms.
Figure 5.2 Frames and time slots.
Radio Transmission

• Physical Channels:
  – Each time slot carries 324 bits, so that the data rate per carrier is $324 \times 6 / 40 \text{ ms} = 48.6 \text{ kb/s}$
  – A full-rate channel can occupy 2 slots (slots 1 and 4, slots 2 and 5, slots 3 and 6) and the bit rate is $16.2 \text{ kb/s}$

• In contrast to AMPS, NA-TDMA has no fixed assignment of physical channels to digital control channels
Figure 5.3  Half-rate physical channel (one slot per frame) and full-rate physical channel (two slots per frame).
Radio Transmission

• Modulation:
  – The modulation format for the 48.6 kb/s is $\pi/4$ shifted DQPSK (differential quaternary phase shift keying)
  – DQPSK is a four level modulation scheme, each transmitted signal referred to as a channel symbol, carries 2 bits to receiver
  – For each symbol, the possible phase changes are odd multiples of $\pi/4$
  – The modulation efficiency is $48.6 \text{ kb/s} / 30 \text{ kHz} = 1.62 \text{ b/s/Hz}$
Figure 5.4 $\pi/4$ shifted differential quaternary phase shift keying. (Reproduced under written permission from Telecommunications Industry Association.)
Radio Transmission

• Radiated Power
  – NA-TDMA specifies 11 power levels for terminals

• Spectrum Efficiency
  – An all-digital network occupying 25 MHz has 416 carriers and $3 \times 416 = 1248$ full rate physical channel
  – Assume the reuse factor is 7 and control channel is $3 \times 7 = 21$ then the traffic channel is 1227
  – the spectrum efficiency is $E = \frac{1227}{7/25} = 7.01$ conversation/cell/MHz
Logical Channels

• NA-TDMA supports all of the AMPS logical channel in addition to the digital control channels and digital traffic channels specified in IS-136

• A Digital Traffic Channel (DTCH) transmit information in six formats as shown in Fig. 5.5

• Forward Digital Control Channel (DCCH) multiplex information in nine distinct formats, including 3 broadcast control channels and 3 point-to-point channels

• A Random Access Channel is a many-to-one channel carrying message from terminal to a BS
Figure 5.5 NA-TDMA logical channels.
Logical Channels

• Digital Traffic Channel (DTCH)
  – Fig. 5.6 displays the contents of each time slot in a DTCH
  – Three terminals share the same carrier and it is important to prevent their signals from arriving at the BS simultaneously
  – A 6-bit guard time (G): to prevent the signal interference between slots
  – A 6-bit ramp time (R): to come up the power level
Frame
1,944 bits in 40 ms (48,600 b/s)

Slot 1 | Slot 2 | Slot 3 | Slot 4 | Slot 5 | Slot 6

Reverse (Terminal to Base)

G 6  | R 6  | DATA 16 | SYNC 28 | DATA 122 | SACCH 12 | DVCC 12 | DATA 122

Forward (Base to Terminal)

SYNC 28 | SACCH 12 | DATA 130 | DVCC 12 | DATA 130 | DL 11 | RSVD 1

G: Guard time, R: Ramp time
RSVD: Reserved for future use
Logical Channels

• DTCH
  – Terminal can transmit a *shortened burst* when they acquire a new physical channel
  – A shortened burst has a guard time with a duration of 50 bits
  – A shorten burst consists of repeated transmissions of the DVCC and SYNC fields
  – While the terminal transmits a shorten burst, the BS determine the correct timing for the terminal
Logical Channels

- Synchronization Bits (28 bits)
  - It serves two purposes: to synchronize and to train an adaptive equalizer
  - The forward and reverse time slots are offset by 1.9 ms as shown in Fig. 5.2

- Digital Verification Color Code (DVCC)
  - DVCC serves the same purpose as SAT in AMPS
  - Each DVCC is represented by an 8-bit word with (12,8:3) error correcting block code
Logical Channels

- Slow Associated Control Channel (SACCH)
  - is an out-of-band signaling channel
  - the bit rate is \( 2 \times 12 / 0.04 = 600 \text{ b/s} \) in a full-rate physical channel
  - the corresponding logical channels in AMPS are the FVC and RVC and they are in-band signaling channels which interrupt user information each time they carry a message
  - 132 bits (11 time slots) comprise a code word
  - the code word contains a 50-bit network control message protected by an error-detecting cyclic redundancy check (CRC) code and error-correcting code
Logical Channels

– Use a diagonal interleave to spread the 132 bits over 12 transmission time slots

Figure 5.12 Error protection on the slow associated control channel.
(2) place new bits on the diagonal of a $12 \times 12$ matrix
(71' indicates bit 71 in previous code word)

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(3) transmit bits in the first column of the matrix

| 71' | 82' | 93' | 104' | 115' | 126' | 5 | 16 | 27 | 38 | 49 | 60 |

(4) shift the matrix one column to the left

(5) arriving bits

| 72 | 73 | 74 | 75 | 76 | 77 | 78 | 79 | 80 | 81 | 82 | 83 |

Figure 5.13 Diagonal interleaving on the slow associated control channel.
Logical Channels

• Digital Control Channel Locator (DL)
  – The 11-bit DL field contains a 7-bit digital locator value protected by an (11,7;3) error-correcting code

• Fast Associated Control Channel (FACCH)
  – the transmission time on an SACCH is 240 ms
  – for some control function this delay is unacceptable
  – NA-TDMA also incorporates an in-band signaling channel
  – it transmits a 260-bit code word with 49 bits message
Logical Channels

- The transmission time is 40 ms on a full-rate channel.
Logical Channels

• Digital Control Channel (DCCH)
  – Block = 3 Slots = 20 ms
  – Superframe = 32 blocks = 0.64 sec
  – Hyperframe = 2 superframes

• The structure of each DCCH time slot
  – In the reverse time slot, there are 40 bits of additional sync information relative to the DTCH
    • 16-bit preamble that replace the 16 data bits of DTCH
    • 24 bits SYNC+ replaces the DVCC and SACCH of a reverse DTCH
Figure 5.15: Slots, blocks, superframes, and hyperframes on the DCCH.
Logical Channels

- In the forward time slot
  - 12-bit SFP (Superframe phase): inform terminals of the location of the current block
  - 22-bit SCF (Shared Channel Feedback):
    - A busy/reserved/idle (BRI) indication (6 bits)
    - A received/not-received (R/N) indication (5 bits)
    - A coded partial echo (CPE, 11 bits) it carries the least significant 7 bits of the directory number
Logical Channels

• Multiplexed Logical Channels on the Forward DCCH
  – Fast broadcast control channel (F-BCCH)
  – Extended broadcast control channel (E-BCCH)
  – Short message service broadcast control channel (S-BCCH)
  – Short message service, paging, and access response channel (SPACH)
  – Each superframe begins with the F-BCCH and ends with SPACH
Logical Channels

Figure 5.16 Logical channels in a digital traffic channel superframe.
Logical Channels

• Paging Channel Operation, Sleep Mode
  – Paging consumes the terminal power
  – NA-TDMA makes it possible for terminal to recognize paging in sleep mode
  – Paging message arrive in the SPACH blocks of each superframe
  – the number of paging subchannels is a parameter, PEN, range from 1 to 96
  – With PEN = 1, there is only one paging subchannel that occupies all hyperframes
  – With PEN =96, a subchannel appears once in 96 hyperframes
Logical Channels

- There is a hyperframe counter in the BCCH that informs terminals of the current paging subchannel
- Each terminal listens to an assigned subchannel which is determined by a hashing function with MIN

• RACH Access Protocol
  - There are two modes of transmission on the RACH, random access and reserved access
  - In the random access mode, terminal waits for an IDLE indication in the BRI bits of a forward DCCH time slot. The terminal then transmits its information in a specified slot of the reverse DCCH
Logical Channels

– The BS indicates a successful result by means of a BUSY indication in the BRI bits, a RECEIVED indication in the R/N bits, and the final 7 bits of the mobile ID in the coded partial echo
– Failing to receive a successful indication, the terminal waits a random time then try again
– In the reserved mode, the BS put a RESERVED indication in the BRI bits and the last 7 bits of the mobile ID in the CPE portion of the SCF
Logical Channels

• Data Fields of the DCCH
  – Variable length header
  – Variable length information
  – 16-bit CRC
  – 5 tail bits